Overview of the Processors

The SLC 500 processor product line offers four types of chassis-based processors.

SLC 5/01™ Processor (Catalog Number 1747-L511 or 1747-L514)

The SLC 5/01 processor offers the instruction set of the SLC 500 fixed controller in a modular hardware configuration. The SLC 5/01 processor provides:

- two choices of program memory size – 1K or 4K instructions
- control of up to 256 local I/O
- powerful ladder logic programming instruction set
- subroutines
- a DH-485 communication channel (peer-to-peer communication response to message commands only)
- capacitor backup for the -L511; battery backup for the -L514

SLC 5/02™ Processor (Catalog Number 1747-L524)

The SLC 5/02 processor expands beyond the SLC 5/01 processor capabilities by offering additional instructions, increased diagnostics, and peer-to-peer communication options. The SLC 5/02 processor provides:

- PID – used to provide closed loop process control
- indexed addressing
- control of up to 480 local I/O, expandable via Remote I/O and DeviceNet
- program memory size of 4K instructions
- interrupt capability
- user fault routines
- built-in DH-485 communication channel (initiation of peer-to-peer communication)
- ability to handle 32-bit signed math functions

Specifications

The following table summarizes the detailed specifications for the SLC 500 processor family:

Specification	SLC 5/01 (1747-L511, -L514)	SLC 5/02 (1747-L524)	SLC 5/03 (1747-L532)	SLC 5/04 1747-L541	SLC 5/04 1747-L542	SLC 5/04 1747-L543
Program Memory	1K or 4K Instructions	4K Instructions	12K Words	12K Words	28K Words	60K Words
Additional Data Storage	0	0	up to 4K Words	up to 4K Words	up to 4K Words	up to 4K Words
Max. Local I/O Capacity	256 Discrete	480 Discrete	960 Discrete	960 Discrete	960 Discrete	960 Discrete
Remote I/O	NA	Maximum number dependent on system power supply loading and program memory size. (4096 inputs and 4096 outputs)				
Max. Local Chassis/Slots	3/30	3/30	3/30	3/30	3/30	3/30
Programming	PLC-500 A.I., APS, and HHT	PLC-500 A.I., APS, and HHT	PLC-500 A.I. and APS	PLC-500 A.I. and APS	PLC-500 A.I. and APS	PLC-500 A.I. and APS
Programming Instructions	52	71	99	99	99	99
Typical Scan Time ①	8 ms/K	4.8 ms/K	1 ms/K	0.9 ms/K	0.9 ms/K	0.9 ms/K
Bit Execution (XIC)	4 µs	2.4 µs	0.44 µs	0.37 µs	0.37 µs	0.37 µs

① The scan times are typical for a 1K ladder logic program consisting of simple ladder logic and communication servicing. Actual scan times depend on your program size, instructions used, and the communication protocol.

The following table summarizes the communication options for the SLC 500 processor family.

Communication	Receive	Receive or Initiate
DH-485	SLC 5/01	SLC 5/02, SLC 5/03, SLC 5/04
RS-232 (DF1 Full-Duplex, DF1 Half-Duplex Master/Slave, DH-485, or ASCII)	SLC 5/01 ①	SLC 5/02, ① SLC 5/03, SLC 5/04
Data Highway Plus	SLC 5/01 ②③	SLC 5/02, ②③ SLC 5/03, ② SLC 5/04

① A 1747-PIC is required when connecting to the DH-485 channel.

② A 1785-KA5 is required.

③ Receive is only through the 1785-KA5.